PL-TR-
97-1151

A STUDY OF ADVANCED SEMICONDUCTOR SWITCH PHYSICS AND TECHNOLOGY

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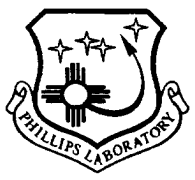
September 1997

Final Report



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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 074-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	September 19, 1997	Final, September 1994 - September 1997

4. TITLE AND SUBTITLE
A Study of Advanced Semiconductor Switch Physics and Technology

5. FUNDING NUMBERS
Contract No.
F29601-94-K-0195
PE:62601F
PR:5797
TA:AK
WU:BC

6. AUTHOR(S)
E. Schamiloglu, C.B. Fleddermann, R. Focia, and J. Gaudet

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The University of New Mexico
Department of Electrical & Computer Engineering
Albuquerque, NM 87131-1356

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Phillips Laboratory/WSQW
3550 Aberdeen Ave SE
Kirtland AFB, NM 87117-5776

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
PL-TR-97-1151

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT ***(Maximum 200 Words)***

Russian ultra-fast, solid state switch technology was investigated in this study. Drift step recovery diodes (DSRDs) with silicon avalanche shapers (SASs) were experimentally examined. In addition, the SAS was studied using device-level modeling. The experiments and model results were compared with each other and with the Russian theory of operation. This research demonstrated that the Russian theory of the SAS was inconsistent with the operational behavior and circuit simulation. The SAS operates in a manner more consistent with a TRAPATT (TRApped Plasma Avalanche Triggered Transit) device. A simple circuit used to test the DSRD and SAS device is presented. Lifetime test results and switching voltage waveforms are discussed and evaluated. An optimum design for the SAS is offered based upon the theory of operation and code simulations. The University of New Mexico's drift diffusion furnace was used to construct a series of avalanche shapers similar in behavior to the Russian SAS. The results of this effort, including experimental data, are presented. Finally, a variety of commercialization opportunities for this fast semiconductor switch technology is offered.

14. SUBJECT TERMS
subnanosecond switch, silicon avalanche switch, drift step recovery diode, silicon avalanche shaper, Russian solid state switch, TRAPATT devices

15. NUMBER OF PAGES
48

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

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I. Introduction

1. Background

This report summarizes the detailed study conducted by the University of New Mexico on advanced semiconductor switch physics and technology. During this study, important, new data was collected on the Russian high-power solid-state switch technology pioneered by Igor F. Grekov [1, 2, 3] and his colleagues at the Ioffe Physical-Technical Institute (to be referred to as the Ioffe Institute in the rest of this report) in St. Petersburg. In addition, a new understanding of how these devices operate was developed, and a design for the pulse shaping diode based on computer simulations was successfully built and tested for comparative analysis.

The Air Force has an interest in very fast, subnanosecond switches that are capable of commutating high power (i.e., high voltage, 100s' of kilovolts) for its pulsed power needs in various applications. In addition to high power, fast repetition rate is also desirable. To accomplish this, one of the technologies that has been under study for several years within the Air Force and the other DOD components is fast switching with photoconductive solid state devices using a light-sensitive material such as gallium arsenide (GaAs) [4]. However, although high switching voltages (123 kV) and fast rise times (200 ps) have been achieved [5], this approach has suffered from two major drawbacks. First, the lifetime of these devices has been suspect, probably due to the fact that the switching process inherently produces filamentation (narrow channels of high current) through the bulk material of GaAs. Consequently, damage to the semiconductor occurs rapidly (after only 10^6 to 10^7 shots) [5]. Second, this type of switch requires the use of a small laser to trigger the avalanche process. This complicates the circuit design and can be a source of much larger required seed energy for the system.

The Ioffe group in St. Petersburg, Russia, reported starting in 1979 and continuing through the decade of the 1980s the development of a new principle of silicon-based solid-state switching [[1], [6]]. They indicated that a variety of devices (diodes, transistors, thyristors, etc.) could be manufactured using specially doped silicon and carefully designed circuits. In addition, using tiny "shaper" heads, a high power closing switch with a closing time of initially < 500 ps (improved to 50 ps in later years) for voltages of several kilovolts had been demonstrated. Each switch also could be timed to within 50 ps, suggesting that many of these assemblies could be stacked together to obtain very high voltages and power.

2. Research Overview

The University of New Mexico proposed to acquire and study actual Russian devices and their technology for the Air Force. A three-year effort was agreed to. The following summarizes the work to be accomplished in each of the three years.

Year 1: Acquire switches, both Russian and U. S. manufactured. Design and build test circuits to validate the switch parameters and technology. Begin to outline the parameter space that affects the performance of the switches. Begin to identify modeling capabilities relevant to the acquired switches.

Year 2: Continue work to identify the critical parameters that yield successful operation of the devices. Modeling of the devices will proceed in conjunction with the experiments. Initiate attempts at fabricating devices and subdevices.

Year 3: Attempt in-house fabrication of comparable devices based on the understanding gained in years 1 and 2 in order to verify the models and hypotheses developed.

The results of Years 1 and 2 of this research have already been reported in detail in various oral presentations, technical articles, quarterly status reports, and interim annual reports. Many of these references appear in the bibliography at the end of this report. The purpose of this final report is to summarize these results, highlighting the work accomplished in Year 3, list the conclusions, and make recommendations for future work.

This final report is organized in the following manner: the next chapter will discuss the experimental results obtained using the Russian switches. Then, the modeling effort for the operation of these devices is presented in Chapter III. Recommended design approaches are discussed in Chapter IV. The degree of our understanding how these switches operate largely depends on our ability to fabricate similar devices ourselves. A description of the fabrication process to make the fast diodes and the UNM techniques employed are presented in Chapter V. The test results of the UNM-fabricated switches are given in Chapter VI. Dual use opportunities for this technology, especially commercial applications, are mentioned in Chapter VII. Finally, conclusions and recommendations about this research are given in Chapter VIII.

II. Russian Switch Experimental Results

1. Tasks.

The experimental tasks to assess the performance of the Russian switch components are: (a) acquire the switches from the Ioffe Institute in St. Petersburg, Russia, (b) design and build test circuits to operate these switches to confirm their published operating parameters and lifetime, and (c) outline the parameter space that affects performance of the switches. This latter task will be discussed in Chapter III and IV since in this project, the best operation of these devices was determined through both experiment and modeling.

1.1 Switch Acquisition

The two different types of switches that were studied in this research project were drift step recovery diodes (DSRDs) and silicon avalanche shapers (SASs). The DSRD and SAS are both silicon-based, two-terminal, p^+-n-n^+ structures. The University of New Mexico acquired from Russia 20 type I (slow type) DSRDs, 10 type II (fast type) DSRDs (both rated at 2.5 kV), and 20 SASs (to match type II DSRDs). This process was done through Moose Hill Enterprises, Inc.[1] which has the exclusive rights to negotiate contracts in the U. S. for the Ioffe Institute and its main high power, fast switch developers, Igor F. Grekhov and Alexei Kardo-Sysoev. The DSRDs thus obtained were 2.5 kV solid state opening switches with anticipated rise times of 2 – 5 ns with a lifetime greater than 1 x 10^{11} shots. The faster type II DSRDs have a reported rise time of 0.5 – 1.5 ns at the same voltage as the type II and with the same lifetime. The SASs received were matched to the type II DSRD with an advertised rise time of less than 100 ps.

A detailed description and brief history of these devices can be found in Ref. 7.

1.2 Design and Build Test Circuits

This task was accomplished successfully and documented in a published paper [8]. A block diagram of the experimental setup used to test the DSRD and SAS is shown in Fig. 1. The main components of this test circuit are two HP-8015A pulse generators, two metal-oxide-semiconductor field-effect transistors (MOSFETs), low-loss, mica charging

[1] Moose Hill, Enterprises, Inc., 54 Jennie Dade Lane, Sperryville, VA 22740. The U. S. representative for these Ioffe Institute switches is Barney O'Meara, (540) 987-8271, e-mail: bom.mhe@mcimail.com

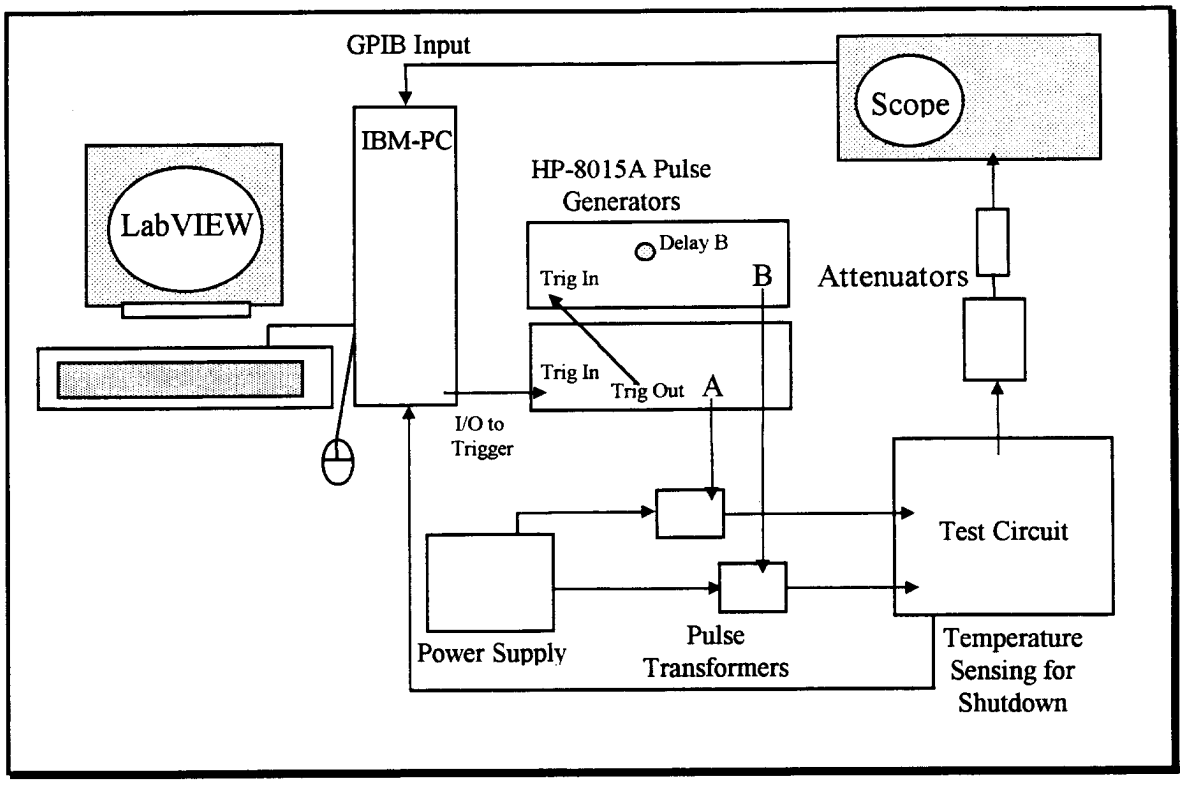

Figure 1. Block diagram of the experiment.

capacitors (assembled in parallel), and two custom-built inductors. For diagnostics, a Tektronix SCD-5000 transient event digitizer was used to record pulse waveforms.

The basic concept of the circuit is to provide energy to the DSRD by releasing energy from two legs of an R-L-C circuit with appropriate timing being critical. Figure 2 shows the details of this circuit arrangement. Then, to get the DSRD to act as a fast opening switch, the turn-off behavior of a DSRD is exploited. The SAS shaper head device is added to the main circuit with the DSRD (See Fig. 3). This small device sharpens the pulse to get extremely fast switching times, less than 100 ps. With the SAS in the test circuit, the output of the DSRD pulse generator is capacitively coupled to the reverse-biased SAS to eliminate dc bias effects. In the test circuit, the desired output pulse voltage is set by varying the supply voltage. One must be careful not to exceed the component rated values else flat-topped, saturated pulse will result.

For more details on this test circuit design see Refs. 8 and 9.

2. Experimental Results

The end result of the experimental portion of this research project was to compare the "advertised" switch parameters from the manufacturer; i. e., Ioffe Institute, with the values measured in our laboratory using the test circuit described above. Table 1

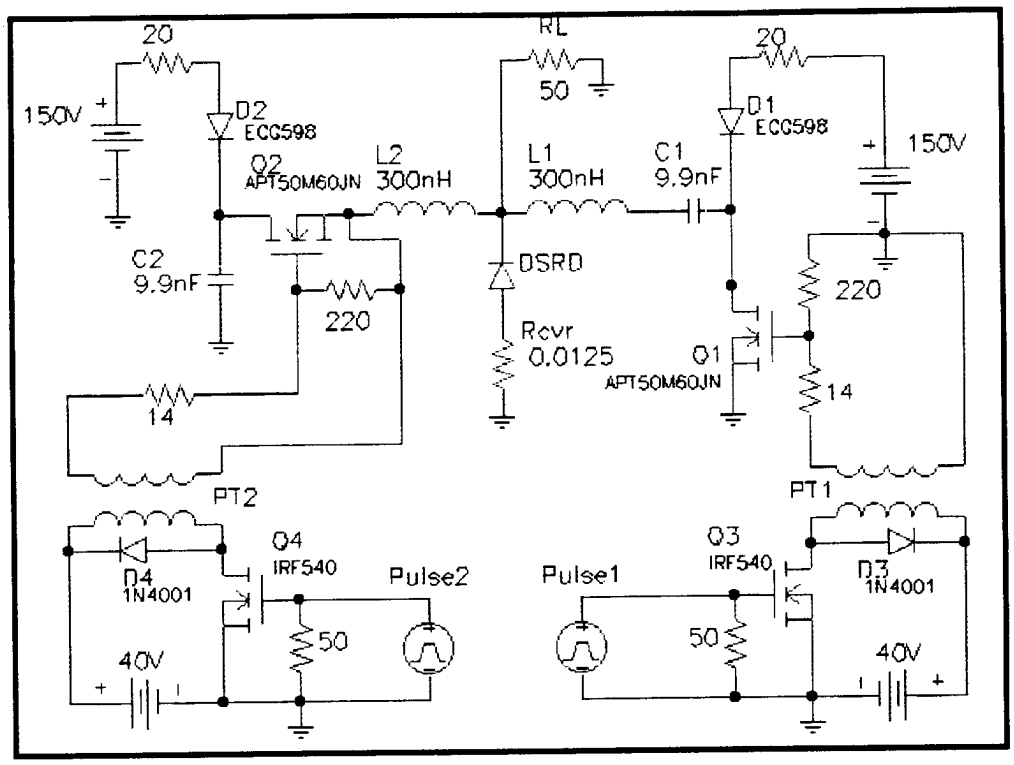

Figure 2. Schematic diagram for the single-stage DSRD pulse generating circuit.

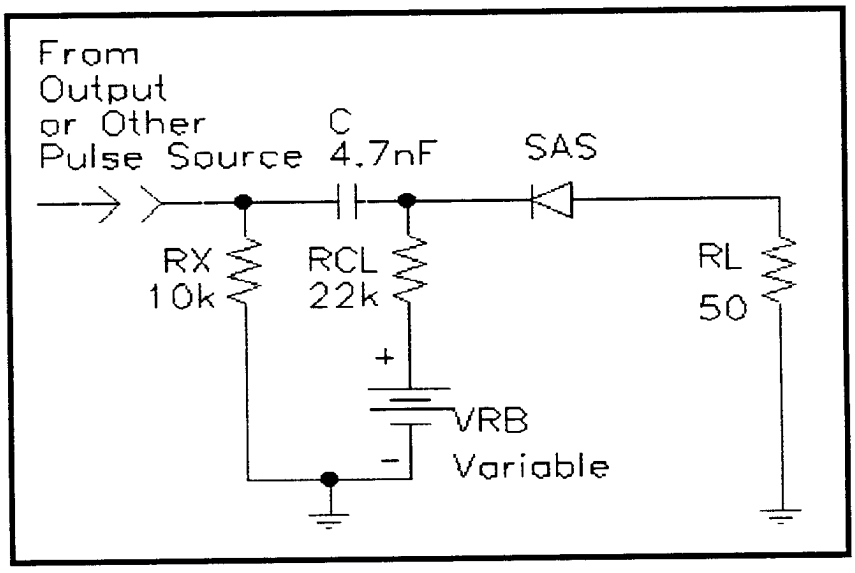

Figure 3. Circuit modification for implementation of the SAS impulse sharpening.

summarizes the results of these experiments for both the DSRDs and SASs tested. Note that due to circuit limitations, the optimum dV/dt of ~ 10^{12} V/s was not achieved. The value of ~ 6 x 10^{11} V/s fell short of ideal; this probably explains the greater than advertised switch times observed for the SAS.

2.1 Drift Step Recovery Diodes (DSRDs)

Both types of DSRDs were extensively tested during this project. The typical waveforms produced by the type I DSRD is indicated in Fig. 4. The waveform for the

Table 1. Comparison of Switch Properties, "Advertised" and Measured.

Parameter		Type I DSRD	Type II DSRD	SAS
Rise time (ps)	*Advertised*	2000 – 5000	500 – 1500	< 100
	Measured	2100	740	450*
Breakdown Voltage (kV)	*Advertised*	2.5	2.5	
	Measured	> 2.9	2.7	
Lifetime (# of shots)	*Advertised*	> 10^{11}	> 10^{11}	Not specified
	Measured	> 10^{11}	> 10^{11}	> 10^{11}

*Tests not conducted at optimum dV/dt

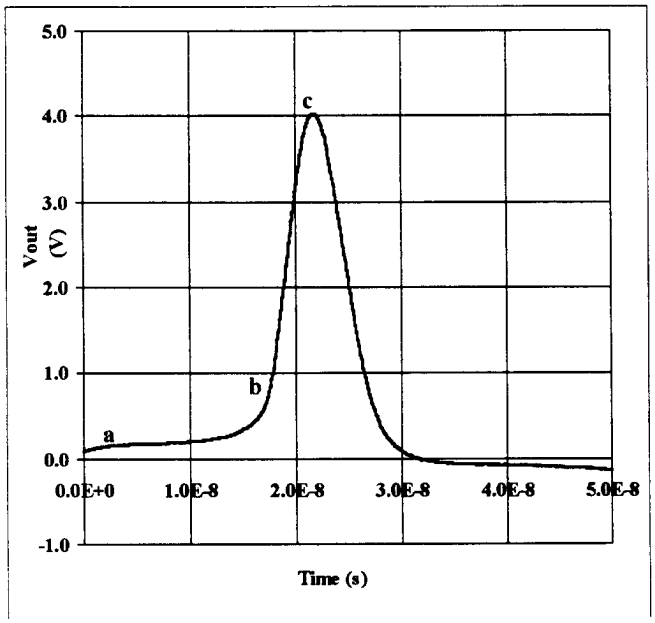

Figure 4. Type I DSRD output pulse. The time scale is 10 ns/div. On the vertical scale, 1 V = 406.7 V.

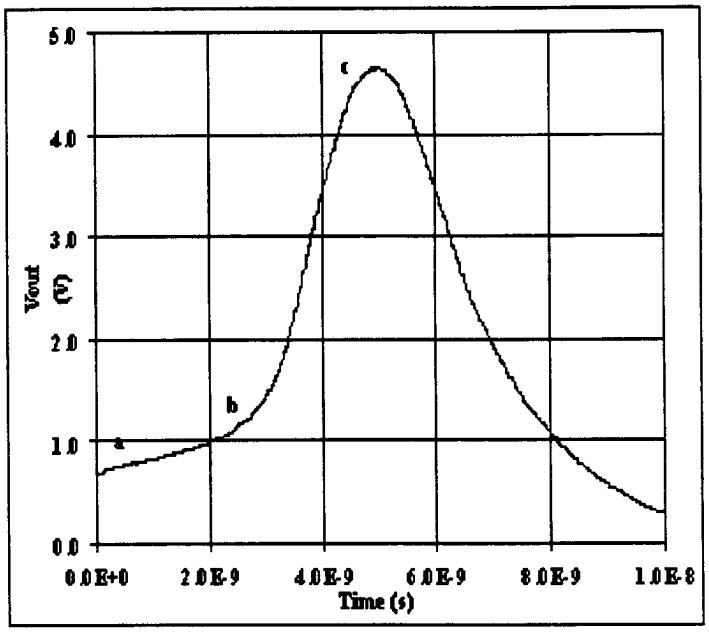

Figure 5. Type II DSRD output pulse. The time scale is 2 ns/div. On the vertical scale, 1 V = 406.7 V.

type II DSRD is shown in Fig. 5. The output pulse in both cases was into a 50 Ω load.

The observed rise time is the actual rise time since sensor and instrument factors were much faster than the observed output signals. The slowly ramping portion of the pulse (from a to b in Figs. 4 and 5) is a function of device parameters and initial charge storage. Note that the peak voltage for the type I DSRD was 1.63 kV and that for the type II DSRD was 1.87 kV. As can be seen from Table I, both types of DSRDs lived up to expectations in that they met, or exceeded, expected values.

2.2 Silicon Avalanche Shaper (SAS)

The DSRD circuit was modified to produce a very fast-rising pulse by adding an SAS coupled to it (Fig. 6). It is reverse-biased through a current limiting resistor and acts as a fast closing switch. The bias may be as low as 10 V or as much as the breakdown

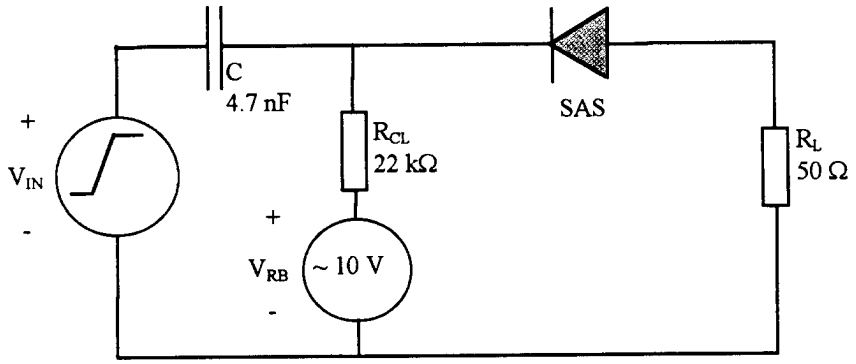

Figure 6. Simplified test circuit implemented in testing and modeling of the SAS.

voltage. Since the optimum performance of the SAS requires a driving pulse with a dV/dt of $\sim 10^{12}$ V/s the DSRD is an ideal match having a theoretical limit for dV/dt at the same value.

A typical output waveform for the test circuit with a type II DSRD shaped with the SAS is shown in Fig. 7. The *dV/dt* for the DSRD for this pulse was $\sim 6 \times 10^{11}$ V/s. From "a" to "b" in the figure, the displacement current in the SAS is building up. The fast transition region from "b" to "c" corresponds to the closing of the SAS. The slower region from "c" to "d" is explained by the fact that, due to the non-optimum *dV/dt* used in the test circuit, the SAS closed prior to the driving pulse reaching maximum amplitude.

As indicated in Table II.1, the SAS had no problems switching in the test circuit over 10^{11} times with no evidence of failure. The maximum repetition rate achieved was 10 kHz.

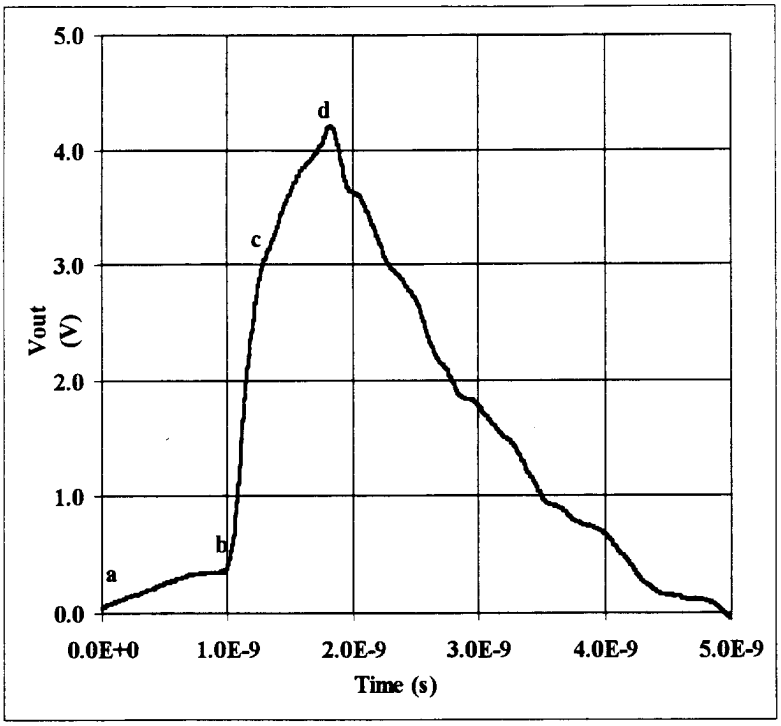

Figure 7. Pulse generated by Type II DSRD and shaped by the SAS. The time scale is 1 ns/div. On the vertical scale, 1 V = 406.7 V.

III. Theory and Modeling of the Silicon Avalanche Shaper

The UNM theory and modeling effort for the Russian solid state switch technology concentrated on the SAS. The reason for this is two-fold. First, the understanding of how this device works was limited. Professor Kardo-Sysoev, co-inventor of this diode, pointed this out at UNM during discussions about this research effort from its inception. Second, the Air Force interest in the Ioffe Institute technology is driven by high power switching needs. Clearly, the faster switching devices (SASs combined with DSRDs) provide the greatest opportunity to obtain the highest powers. Thus, this research project only investigated the physics of the sharpener device, the SAS.

The SASs discussed in this report are silicon-based, p^+-n-n^+ structure two-terminal devices. Figure 8 shows the basic geometry of the SAS with approximate dimensions and doping levels. The breakdown voltage of the device is determined by the dopant concentration and length of the n-region. The maximum current handling capability is determined by Ohmic heating and skin effect issues and can in general be increased by increasing the area of the device to a certain limit.

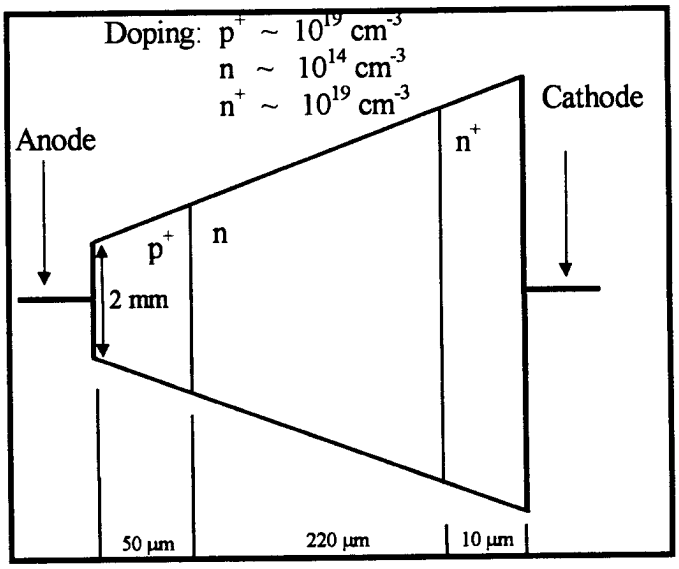

Figure 8. Basic SAS geometry and doping levels according to Russian literature [1].

The device is beveled to prevent premature failure under high reverse bias conditions. The beveling isolates the junction from the edge of the device. The electric field strength will be lower at the beveled edge of the diode compared with the value in the main body [10]. Additionally, beveling the diode separates the contact edges by a larger distance that also reduces the electric field strength between them.

1. *Simplified Theory of SAS Device*

The theory of operation of the SAS as described by Grekhov and colleagues [1], [11] is similar to that of a diode operated in the TRApped Plasma Avalanche Triggered Transit (TRAPATT) mode of operation which has been discussed in numerous articles [[12], [13], [16], [18]]. A simplified review [7] of the theory of an avalanche shock wave is now presented by considering a one dimensional (in x) abrupt junction p^+-n-n^+ silicon structure with a voltage V_A applied. If a steady-state reverse-bias ($V_A < 0$) is applied between the anode and cathode shown in Fig. 8, a small saturation current I_s flows from cathode to anode and the voltage across the device is supported by an electric field E established by a space charge region (SCR). Using the depletion approximation, the

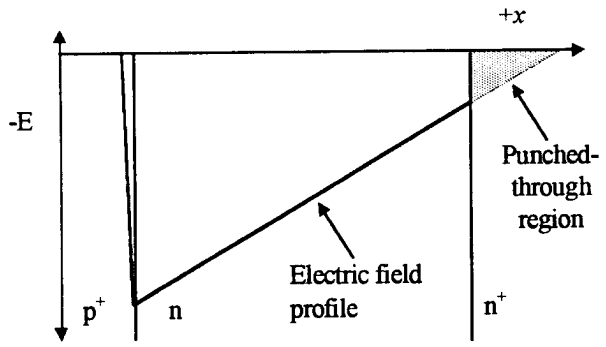

Figure 9. Electric field distribution.

qualitative magnitude and direction of the static electric field distribution for this device in the reverse-biased condition is shown in Fig. 9. The negative amplitude of the electric field implies that it is in the -x direction. The result of an increase in the reverse-bias voltage is an expansion of the SCR into the n- and p^+-regions with a corresponding increase in the magnitude of the electric field at the p^+-n junction. There is also a SCR established at the n-n^+ boundary, the effects of which are neglected here. The distance that the SCR must extend into the n- and p^+-regions to support a given reverse-bias voltage is given by [19]:

$$x_n = \sqrt{\frac{2\varepsilon}{q}(V_{bi} - V_A)\frac{N_A}{N_D(N_A + N_D)}}, \tag{1}$$

and,

$$x_p = x_n\left[\frac{N_D}{N_A}\right] \tag{2}$$

respectively. Here ε is the permittivity of the material (for silicon $\varepsilon = 11.8\varepsilon_o$, where ε_o is the permittivity of free space), q is the electron charge, N_A is the dopant concentration in

the p^+-region, N_D is the dopant concentration in the n-region, V_{bi} is the built-in potential (V_{bi} is usually on the order of 0.5-0.8 V), and V_A is the voltage applied to the diode contacts. The small Ohmic voltage drops due to current flow in the neutral regions of the device are neglected in this analysis. With the dopant concentrations shown in Fig. 8 the SCR extends primarily into the lightly doped n-region and has a slope given by:

$$\frac{\partial E}{\partial x} = -\frac{qN_D}{\varepsilon}. \tag{3}$$

determined from Poisson's equation.

The breakdown voltage V_{BR} of an abrupt PN junction diode is related to its material properties by [19]:

$$V_{BR} = E_c^2 \frac{\varepsilon}{2q}\left[\frac{N_A + N_D}{N_A N_D}\right] \tag{4}$$

where E_c is the critical electric field strength for impact ionization. For the case of the p^+-n junction where $N_A >> N_D$, V_{BR} can be approximated by:

$$V_{BR} = E_c^2 \frac{\varepsilon}{2q}\left[\frac{1}{N_D}\right]. \tag{5}$$

If the length of the n-region is shorter than that necessary to allow the SCR to completely expand to support the applied reverse voltage, the SCR is said to "punch through" [16] the n-n^+ boundary, as shown in Fig 9. For the punched-through diode the breakdown voltage will be reduced by a factor related to the shaded area shown in Fig. 9. To simplify further discussions a punched-through structure is assumed.

If a constant-amplitude current density J_o is applied to the punched-through diode in the reverse direction the current in the n-region will be due entirely to displacement current. Figure 9 shows how the magnitude of the electric field strength will change in the n-region with time for this situation.

The current density in the n-region is given by

$$J_o = \varepsilon \frac{dE}{dt}. \tag{6}$$

If $E = E_c$ at the p^+-n junction when $t = t_o$, the electric field strength can be described by:

$$E(x) = E_c - \frac{qN_D x}{\varepsilon}. \tag{7}$$

Since J_o is assumed constant, the time varying electric field strength is given by:

$$E(x,t) = E_c - \frac{qN_D x}{\varepsilon} + \frac{J_o t}{\varepsilon}. \tag{8}$$

The intercept point where $E(x, t) = E_c$ is given by:

$$\frac{qN_D x}{\varepsilon} = \frac{J_o t}{\varepsilon}. \tag{9}$$

The velocity of this intercept point can be found by taking the derivative of Eq. (9) and is given by:

$$v_{IW} = \frac{dx}{dt} = \frac{J_o}{qN_D}. \tag{10}$$

Equation (10) implies that an avalanche shock front can be generated that has a velocity greater than the saturated carrier velocity v_s. This shock front can be thought of as an ionization wave that propagates through the n-region leaving in its wake a highly conductive electron-hole plasma. If the diode is driven with a current density such that the electric field grows faster than carrier generation due to impact ionization can respond to reduce the field, there can be a region where $E > E_c$ resulting in a delayed breakdown effect. The critical requirement in generating the ionization wave is

$$J_o > J_{\min} = v_s qN_D \tag{11}$$

where v_s is the saturated carrier velocity. For a dopant concentration $N_D = 1 \times 10^{14}$ cm^{-3} and $v_s = 1.1 \times 10^7$ cm/s the minimum required current density is $J_{min} = 176$ A/cm^2. The applied current density does not have to be constant provided that it exceeds the minimum indicated in Eq. (11).

The ionization wave terminates at the n-n$^+$ boundary leaving the entire n-region filled with a dense electron-hole plasma. The rate at which the device can switch current is determined by the impact generation rate and is on the order of tens of picoseconds. The amount of current that is switched before the diode voltage is restored depends on the external resistance of the circuit, the length of the n-region, and the area of the device.

Experimental data has shown that the SAS exhibits this rapid current switching behavior when a voltage pulse applied in the blocking direction has a $dV/dt \geq 2 \times 10^{12}$ V/s [[1], [11]]. For an applied pulse with a constant dV/dt the displacement current in the n-region is given by:

$$J_d = \frac{qN_D}{2}\frac{dV_A}{dt}\sqrt{\frac{2\varepsilon N_A}{qN_D(N_A + N_D)}}\frac{1}{\sqrt{V_{bi} - V_A(t)}}. \tag{12}$$

For the dopant concentrations shown in Fig. 1(a), $dV_A/dt = 2 \times 10^{12}$ V/s, and $V_A(t) = -1000$ V, the displacement current density is $J_d = 183$ A/cm^2. This value exceeds the minimum required by Eq. (11). Since the applied voltage is increasing with time J_d will decrease accordingly. The result of Eq. (12) is that a mode of operation similar to that of the TRAPATT can be achieved with an appropriately manufactured device if the applied voltage pulse has a sufficiently large *dV/dt*.

2. *Comparison of Russian Theory of the SAS with Simulation/Models/Experiment*

One of the major goals of this research was to generate a higher level of understanding as to how the SAS devices work. This not only included conducting the experiments described in Chapter II but also reviewing the existing Russian theory of operation, and creating new concepts of operation where necessary and possible. The last section described a simplified theory of the SAS that is essentially that of a TRAPPAT-like device. In this section, we discuss how the Russian theory [[1], [6], [11]] which has been accepted since the early 1980s can be analyzed based upon code modeling and the experiments discussed earlier.

2.1 Russian Theory of the SAS

Grekhov and colleagues consider a device that is not punched-through so that the SCR developed by the reverse-bias voltage can fully extend into the n-region. In this case, the n-region consists of a SCR and a quasineutral region (NR). The current density in these regions is given by:

$$J = J_c + J_d = \sigma E + \varepsilon \frac{\partial E}{\partial t} \tag{13}$$

where J_c is the conduction current density, J_d is the displacement current density, and σ is the conductivity of the particular region. The conductivity of the n-region is given by

$$\sigma = \frac{1}{\rho} = q\mu_n N_D \tag{14}$$

where ρ is the resistivity and μ_n is the carrier mobility. Their theory of operation of the SAS is essentially the same as that of the TRAPATT mode of operation until the ionization wave starts to propagate into the n-region. Here, they state that if the SCR does not overlap the entire n-layer (i.e. the device is not punched through), the overvoltaged region (region where $E > E_c$), when displaced into the NR, is uniform. What they mean by this is that when the ionization wave starts to propagate, the electric field strength in the entire NR instantaneously becomes greater than E_c. Due to the high

concentration of carriers ($n = N_D$) ionization starts in all of the NR simultaneously and the entire NR is filled by an electron-hole plasma very quickly as previously seen in the SCR. As the electron-hole plasma is formed in the SCR the electric field is reduced in that region. The reduction in electric field causes the voltage across the diode to be reduced. Circuit theory predicts that the load voltage (Fig. 4) must increase, and thus, current must flow in the load. The increase in load current also causes an increase in the current density in the diode. This implies that the electric field in the NR will increase as predicted by Eq. (13).

However, the current density necessary to achieve $E > E_c$ in the NR is at a minimum one order of magnitude greater than that predicted by circuit theory and the area of the SAS diodes used in our experiments. This was confirmed by observation of the NR electric field magnitude in the baseline computer modeling [[9] and section 2.3 of this chapter].

2.2 SAS Circuit Simulation and Comparison with Experiment

The SAS circuit was modeled using a commercial software package from Silvaco International including ATLAS, ATHENA and other tools.[2] Besides allowing the user to input circuit elements like voltage sources, capacitors, and resistors, it permits the semiconductor elements to be modeled in two dimensions. The current and voltage for such devices uses a solution to Poisson's equation and the continuity equations for electrons and holes. Various secondary equations for the current densities, charge generation rates and recombination rates are also solved. The charge transport model chosen for this simulation was the simplest available, a drift diffusion model.

The published values for the SAS [[1], [11]] were used in a baseline simulation using the circuit as illustrated in Fig. 2, and 3 (or Fig. 6). The results of the numerical model were inconsistent with the experimental data. Figure 10 shows the results of the baseline calculation. The thickness of the n-region was assumed to be 220 μm and an applied voltage dV/dt of 6×10^{11} V/s. This simulated curve should be compared with Fig. 7. In Fig. 10 there is a region where displacement current in the device causes the load voltage to be greater than zero as predicted. This region is followed by a rapid transition in load voltage. There is a large disparity between the load voltage and the input voltage at the peak of this rapid transition phase. For a short time period after the rapid transition phase the load voltage decreases and then increases at a rate comparable to that in the

[2] SILVACO International, 4701 Patrick Henry Drive, Bldg. 1, Santa Clara, CA, 94054. Telephone (408) 567-1000. Internet site: http://www.silvaco.com.

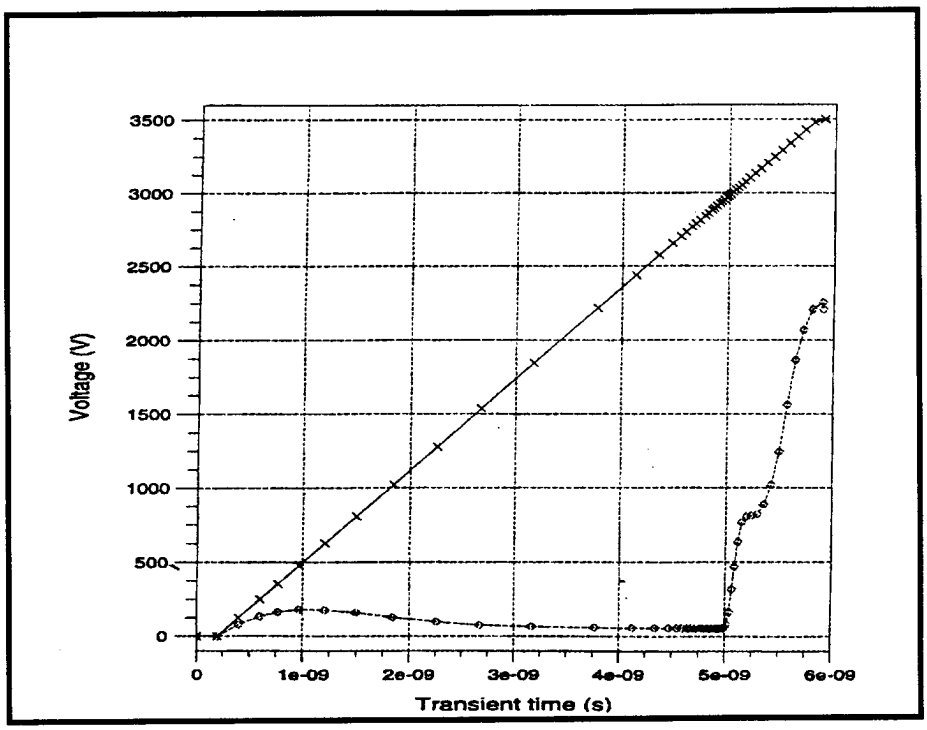

Figure 10. Input and load voltage for the baseline simulation

initial rapid transition phase. A similar cycle appears to be forming after this second rapid transition phase. An explanation for this behavior is given by describing the electric field in the structure at the times corresponding to the diamond markers on the load voltage waveform shown in Fig. 10. Under reverse-bias conditions, the diode voltage is maintained by the electric field in the device. If the device is driven with a sufficient current density in the reverse direction (Eq.(12)) then the diode voltage may exceed the breakdown voltage for a short period of time. This also implies that there is a region where the electric field strength is greater than the critical electric field strength E_c. After a delay time on the order of tens of picoseconds, impact ionization generates an electron-hole plasma with a sufficient density that a significant region of the electric field is quenched. The electric field is quenched on a time scale consistent with the impact generation rate that is also on the order of tens of picoseconds. A quenching of the internal electric field of the device will reduce its terminal voltage accordingly. Circuit theory predicts that the load voltage must increase to accommodate the reduced voltage across the SAS and current must flow in the circuit (Fig. 6). Conduction current flow in the device will act to separate the mobile electron and hole carriers and restore the internal electric field structure. It is this field restoration that is responsible for the dip in the load voltage in Fig. 10. As the ionization wave (I-wave) moves through the n-region another region where $E > E_c$ is created and the initial cycle is repeated until the I-wave reaches the $n\text{-}n^+$ boundary. As the I-wave propagates through the n-region the electric field strength in the quasi-neutral region increases consistent with the device current and Eq. (13).

2.3 Circuit Simulation Compared to Russian Theory

The result that the electric field increases with device current through the n-region is contrary to the Russian theory [[1], [6], [11]], which suggests that as the ionization wave is initially displaced into the n-region the electric field strength in the entire quasineutral region is elevated to a value in excess of the critical electric field. From this analysis it is clear that in order to reduce the disparity between the input and load voltages after the initial rapid transition phase the length of the n-region must be such that the region where $E > E_c$ consumes the entire n-region. *This implies that a significantly punched-through device is required for optimum performance.*

Additional measurements of the static breakdown voltage were performed on several SAS devices after running the baseline numerical simulation. The measured static breakdown voltage was ~ 1500 V. Consider an increasing reverse-bias voltage on the SAS that corresponds to a widening of the SCR. For an abrupt PN junction diode, the length that the SCR will extend into the n- and p^+-regions is given by Eqs. (1) and (2).

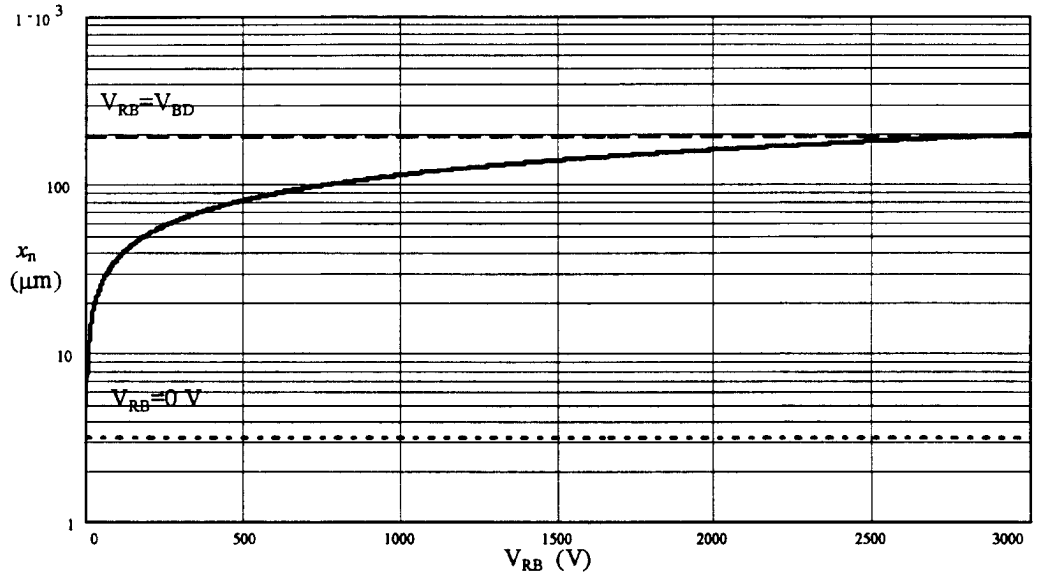

Figure 11. Equation (1) plotted for $N_D = 1 \times 10^{14}$ cm^{-3} versus reverse-bias voltage.

This implies that for the p^+-n junction, the SCR will extend primarily into the n-region. Equation (1) is shown plotted in Fig. 11 for $N_D = 1 \times 10^{14}$ cm^{-3} versus the reverse-bias voltage. This plot confirms a punched through structure for an n-region dopant concentration of 1×10^{14} cm^{-3} and a breakdown voltage of 1500 V. *It is concluded that the length and dopant concentration in the n-region of the actual SAS devices used in this experiment are probably not as described in the literature and not as shown in Fig. 6.*

It was determined that the length of the n-region of the devices used in the experiment was, indeed, shorter than 220 μm based on static breakdown voltage measurements [9].

Following these results, discussions were held with the Russian experimentalists.

Professor Kardo-Sysoev attributes the deviation between their theory and that predicted by the numerical modeling either to possible current filamentation or to the ionization coefficients having a second order dependence on the electric field (i.e. $\alpha = f(E) + f(dE/dt)$) that is much greater than the first order dependence [20]. Extensive fabrication and testing beyond the scope of this work would be required to substantiate this.

2.4 Parametric Studies of SAS Performance Using Circuit Simulation

Computer modeling was performed with the goal of assessing the effect of three parameters on the performance of the SAS. *The three factors determined to most significantly affect the performance of the SAS are the length of the n-region, the dopant concentration in the n-region, and the area of the device.* These studies also suggest that the numerical results differ from the TRAPPAT theory of operation.

Figure 12 shows the input voltage versus the load voltage for the numerical simulation of a SAS with an n-region dopant concentration of $N_D = 1 \times 10^{14}$ cm^{-3} and n-region lengths of 25, 50, 75, and 100 μm. For this dopant concentration the breakdown voltage will depend on the amount of punch through. Equation (1) suggests that at the breakdown voltage the SCR extends ~230 μm into the n-region. The maximum displacement current is on the order of 9 A due to the large area of the device (3×10^6 μm^2). This makes the pre-pulse load voltage small compared to the peak load voltage developed for this device. For large area high-power devices, the pre-pulse voltage could be a significant percentage of the peak voltage developed.

In Fig. 12 there is a rapid rise in load voltage as the electron-hole plasma generated by impact ionization starts to quench the electric field (E-field) in the n-region as discussed previously. The diode voltage that was being maintained by the E-field now decreases on a time scale associated with impact generation rate (tens of picoseconds). For a device with short n-region length (> 50 % punch-through), low n-region dopant concentration, and large area the initial quenching of the E-field can allow the diode voltage to drop to zero and the load voltage to rapidly rise to the input voltage.

In general, the delay time for the device to reach the fully conducting state is governed by the *dV/dt* of the applied pulse and the length of the n-region. The contribution to the delay time after propagation of the I-wave will have a finite limit since the electron-hole plasma developed will decay due to recombination and conduction current flow will reestablish the electric field in the device. With a minority carrier lifetime on the order of 10 μs, the length of the n-region would have to be ~700 cm for recombination to be a problem. This length would make it an impracticably large semiconductor device. Additionally, a longer n-region reduces the amount of conduction current that can flow into the load resistor prior to the restoration of the E-field in the SAS and the formation of a second I-wave. The result is that the length of the n-region cannot be adjusted to arbitrarily increase the delay time without adversely affecting the amount of time the conduction current can flow. The conduction current transient will occur on a much longer time scale if the device geometry is not optimized.

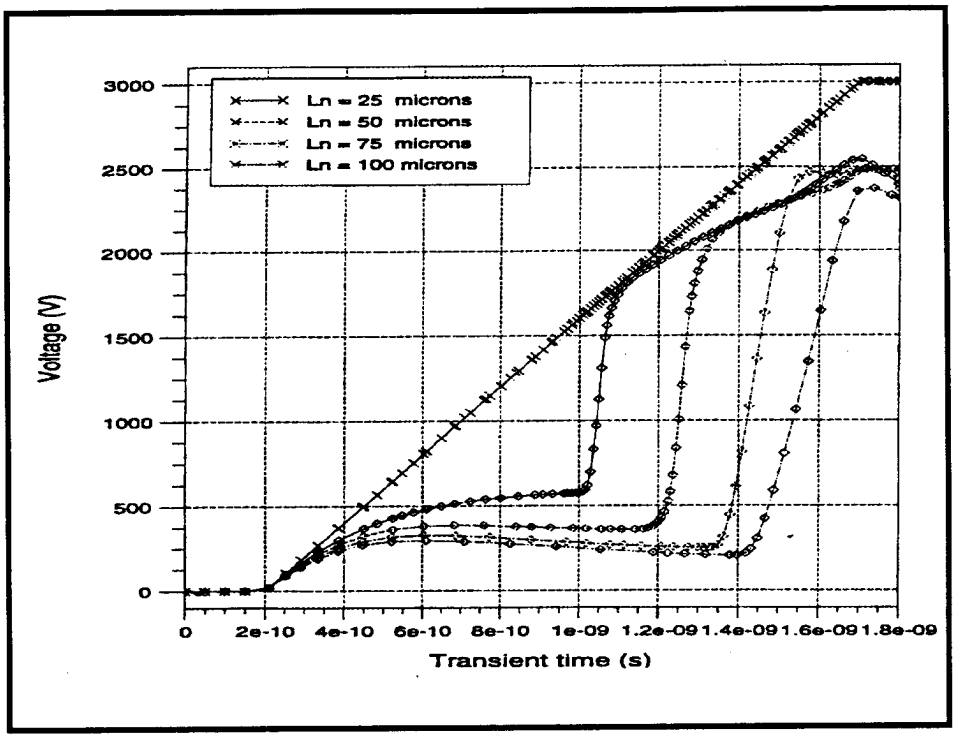

Figure 12. Input versus load voltage for an n-region dopant concentration of 1 x 10^{14} cm^{-3} and n-region lengths of 25, 50, 75, and 100 μm.

The effects of varying the area of a device with an n-region dopant concentration of N_D = 1 x 10^{14} cm^{-3} and length of 75 μm are shown in Fig 13. Note that, as expected, the voltage (power) handling capacity of the device increases with increasing area. The effects of varying the n-region dopant concentration of a device with an n-region length of 100 μm and area of 3.14 x 10^6 μm^2 are shown in Fig. 14.

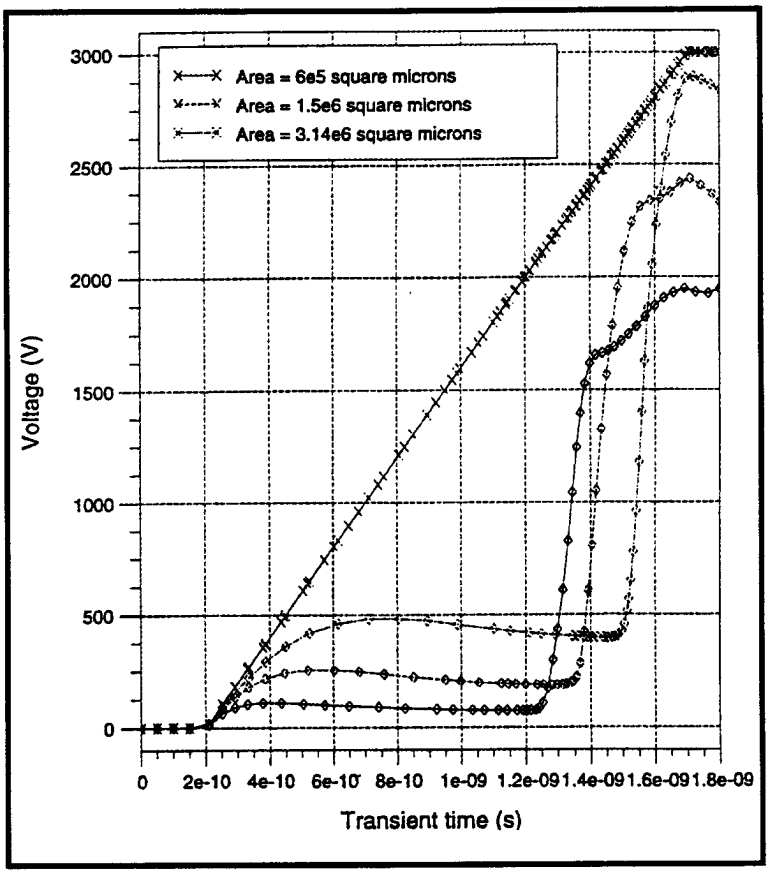

Figure 13. Input versus load voltage for devices of various areas.

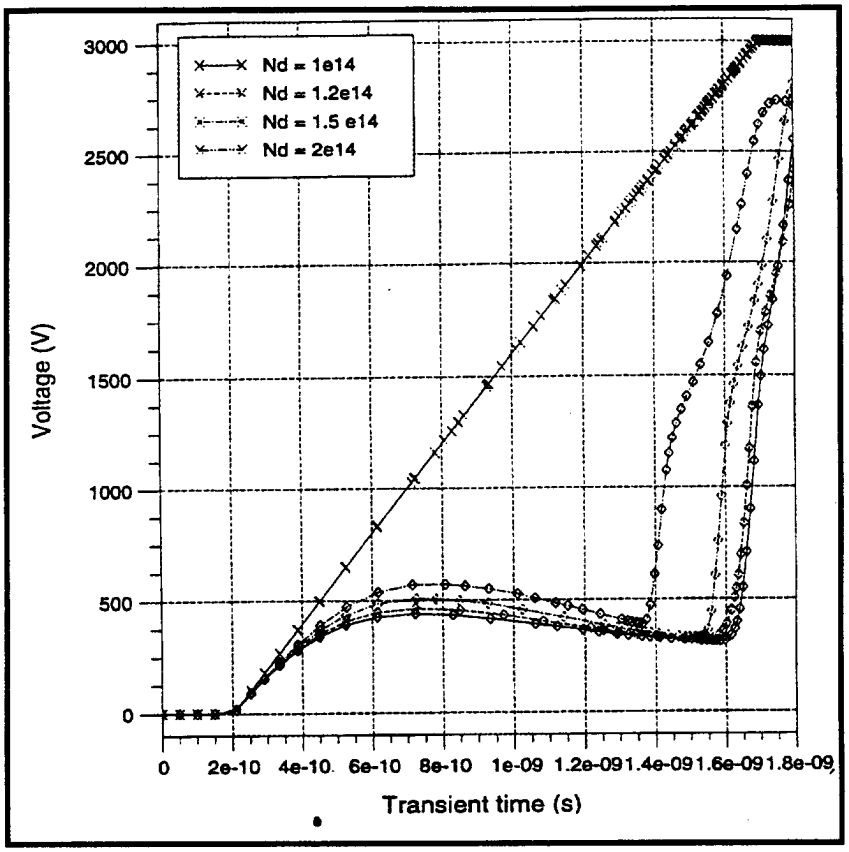

Figure 14. Input versus load voltage for various n-region dopant concentrations

IV. Application of Device Modeling to SAS Design

The purpose of this portion of the research effort was to determine if devices similar in performance to the Russian built SASs could be designed and manufactured using standard U. S. semiconductor practices. The first step in this process is to use the knowledge gained from the operation of the Russian-built SASs and the modeling results of the circuit simulations to optimize the design. Furthermore, testing of these devices are critical for validating our understanding of them.

One optimized design [7] for a pulse sharpening diode is provided in Fig. 15. The ideal SAS would have a high breakdown voltage. This would allow for reducing the

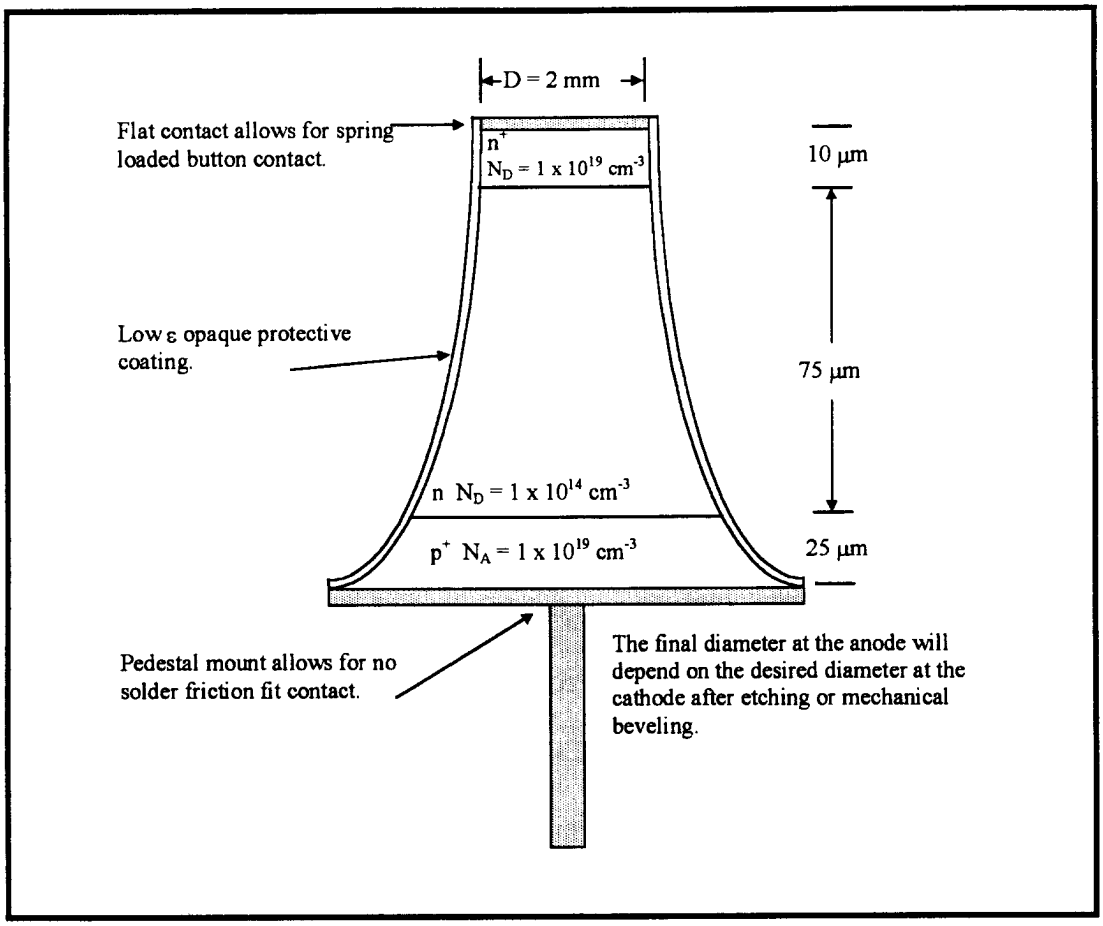

Figure 15. One optimized design for a pulse sharpening diode based on a comparison of experimental data to the results of numerical modeling.

number of devices necessary if they are to be stacked in series to hold off a large reverse-bias voltage. The device should be tapered towards the anode or cathode to prevent premature breakdown under high reverse-bias voltages [21]. The dopant concentration in the n-region should be established first based on the desired breakdown voltage. This dopant concentration will also affect the required *dV/dt* of the input pulse necessary to achieve the current density given by Eq. (12). For these considerations the n-region dopant concentration should be set at the lowest level practicable.

The length of the n-region will depend on the dopant concentration and the desired level of punch through and should be determined by using Eq. (1) or preferably the results of numerical modeling. It is desirable to have a device that is punched-through when the applied reverse-bias is at the expected breakdown voltage in order to maximize the efficiency of power transfer from the input to the load [9].

The length of the p^+- and n^+-regions did not seem to be a factor in the numerical analysis of the SAS but should be much greater than the anticipated SCR thickness in

these regions and also thick enough so that the post-metallization anneal does not allow metal to diffuse near either junction. The values of 25 μm and 10 μm for the p^+- and n^+-regions, respectively, should be adequate. The SAS should be constructed in a "mesa" type geometry from silicon wafers of constant n-type doping in order to facilitate tapering. A constant source diffusion should be performed to generate the p^+- and n^+-regions.

The area of the device will depend on the required power handling capability [12]. For pulse sharpening applications the current flowing through the device will be determined by the load resistance. If the area of the device is insufficient to handle the expected current flow there will be a large disparity between the load voltage developed for a given input voltage. This is due to the conduction current flow and carrier diffusion creating restoring electric fields in the device. Scaling the devices to large areas will increase the prepulse voltage at the load due to displacement current. This prepulse voltage should be small if the load resistance is small but can be significant for large area devices.

The contacts on the devices tested in UNM experiments worked well for mounting in a coaxial insertion unit. The packaging used should eliminate any source of light from reaching the device and also minimize any parasitic effects due to capacitance and inductance.

It should be noted that the proper design of a SAS-type pulse sharpening diode must start with the desired operating parameters. The *dV/dt* of the input pulse must be sufficient to create the required initial current density (Eq. (11)) for the rapid transition mode of operation. The diode geometry combined with the *dV/dt* of the input pulse will determine the time delay before breakdown and the disparity between the input and load voltage at this time.

The design of Fig. 15 is based on an input voltage pulse with a *dV/dt* of 2×10^{12} V/s and peak amplitude of 2300 V. The time delay prior to breakdown will be ~1.15 ns.

V. Fabrication of Fast Switching Diodes

The main effort during the third year of this study was to attempt the manufacture of diodes that exhibit the fast closure properties of the Russian-built SAS. The purpose of this work was to evaluate the computer modeling of the SAS through the careful comparison of a known doping profile of the diode and the modeling tools described elsewhere [9]. Also, if possible, evaluate the optimum design discussed in Chapter IV by constructing a diode to these specifications and running it in the test circuit.

1. General FabricationTechniques[3]

The first step in this process was to construct a diode with a relatively thick active region (about 200 μm) as a check of the methodology and the modeling results. Following the successful test of this diode, a thinner active region diode was built. In both cases, the fabrication process was the same. Manufacturing of a semiconductor may require as many as 100 steps. The process involves the creation of 8 to 20 patterned layers on and into the substrate, ultimately forming the complete integrated circuit. This layering process creates electrically active regions in and on the semiconductor wafer surface. Typical steps consist of the following:

a. *Wafer Production.* This first step in semiconductor manufacturing begins with production of a wafer--a thin, round slice of a semiconductor material, usually silicon. In this process, purified polycrystalline silicon, created from sand, is heated to a molten liquid. A small piece of solid silicon (seed) is placed on the molten liquid, and as the seed is slowly pulled from the melt the liquid cools to form a single crystal ingot. The surface tension between the seed and molten silicon causes a small amount of the liquid to rise with the seed and cool.

The crystal ingot is then ground to a uniform diameter and a diamond saw blade cuts the ingot into thin wafers. The wafer is processed through a series of machines, where it is ground smooth and chemically polished to a mirror-like luster.

The wafers are then ready to be sent to the wafer fabrication area where they are used as the starting material for manufacturing integrated circuits.

b. *Wafer Fabrication.* The heart of semiconductor manufacturing is the wafer fabrication facility where the integrated circuit is formed in and on the wafer. The fabrication process, which takes place in a clean room, involves a series of principle steps Typically it takes from 10 to 30 days to complete the fabrication process.

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[3] This section was largely taken from the Harris Corporation web page, "How Semiconductors are Made," http://rel.semi.harris.com/docs/lexicon/manufacture.html.

c. *Thermal Oxidation or Deposition.* Wafers are pre-cleaned using high purity, low particle chemicals (important for high-yield products). The silicon wafers are heated and exposed to ultra-pure oxygen in the diffusion furnaces under carefully controlled conditions forming a silicon dioxide film of uniform thickness on the surface of the wafer.

d. *Masking.* Masking is used to protect one area of the wafer while working on another. This process is referred to as photolithography or photomasking. A photoresist or light-sensitive film is applied to the wafer, giving it characteristics similar to a piece of photographic paper. A photo aligner aligns the wafer to a mask and then projects an intense light through the mask and through a series of reducing lenses, exposing the photoresist with the mask pattern. Precise alignment of the wafer to the mask prior to exposure is critical. Most alignment tools are fully automatic.

e. *Etching.* The wafer is then "developed" (the exposed photoresist is removed) and baked to harden the remaining photoresist pattern. It is then exposed to a chemical solution or plasma (gas discharge) so that areas not covered by the hardened photoresist are etched away. The photoresist is removed using additional chemicals or plasma and the wafer is inspected to ensure the image transfer from the mask to the top layer is correct.

f. *Doping.* Atoms with one less electron than silicon (such as boron), or one more electron than silicon (such as phosphorous), are introduced into the area exposed by the etch process to alter the electrical character of the silicon. These areas are called p-type (boron) or n-type (phosphorous) to reflect their conducting characteristics.

g. *Repeating the Steps.* The thermal oxidation, masking, etching and doping steps are repeated several times until the last "front end" layer is completed (all active devices have been formed).

h. *Dielectric Deposition and Metallization.* Following completion of the "front end," the individual devices are interconnected using a series of metal depositions and patterning steps of dielectric films (insulators). Current semiconductor fabrication includes as many as three metal layers separated by dielectric layers.

i. *Passivation.* After the last metal layer is patterned, a final dielectric layer (passivation) is deposited to protect the circuit from damage and contamination. Openings are etched in this film to allow access to the top layer of metal by electrical probes and wire bonds.

j. *Electrical Test.* An automatic, computer-driven electrical test system then checks the functionality of each chip on the wafer. Chips that do not pass the test are marked with ink for rejection.

k. *Assembly.* A diamond saw typically slices the wafer into single chips. The inked chips are discarded, and the remaining chips are visually inspected under a microscope before packaging.

The chip is then assembled into a package that provides the contact leads for the chip. A wire-bonding machine then attaches wires, a fraction of the width of a human hair, to the leads of the package. Encapsulated with a plastic coating for protection, the chip is tested again prior to delivery to the customer. Alternatively, the chip is assembled in a ceramic package for certain military applications.

2. UNM Fabrication Process

The major steps used in this research project to fabricate the SAS diodes were:

a. Oxidation: Grow thick enough oxide to mask diffusion of step c). Need about 0.15 μm thick oxide. Wet oxidation at 1100 °C for 1 hour.

b. Etch oxide off of front side in hydrogen fluoride (HF).

c. p^+ diffusion: 2-step diffusion of B, Pre-deposit for 1 hour; drive in 3 hours @ 1100 °C (to get 10^{19} cm^{-3} surface cone and junction depth of 25 μm.

d. Oxidize again. Same condition as step b).

e. Etch oxide off of back side in HF.

f. n^+ diffusion: 2 step diffusion of P, Pre-deposit for ½ hour; drive in 1.5 hours @ 1000 °C (to get 10^{19} cm^{-3} surface cone with 10 μm junction depth).

g. Metalize back and front with titanium.

h. Pattern front side metal into squares.

i. Etch potassium hydroxide (KOH) to define pyramids (stop just before going all the way through, or use higher doping concentration for natural etch stop).

j. Dice (due to thinness, manually break wafer).

k. Attach leads with conducting epoxy.

VI. Testing of UNM-Fabricated Switches

1. Introduction

The test circuit described previously (Chapter II, Section 1.2) was used to test and compare the diode switches that were manufactured according to the prescription outlined above. That is, the newly built diodes were inserted into the circuit of Fig. 3 in place of the SAS. This chapter reports the results of these preliminary tests and compares these results with the Russian switch performance.

An incremental approach was used in building the diodes. The initial batch of diodes was made from a 500 μm wafer thickness of n-type material. Once several of these devices were characterized in the test circuit, thinner material was used in the manufacturing process. Thus, the second batch of diodes had a active region thickness of 250 μm.

2. Results of Samples

A batch of 508 μm thick samples was prepared using the procedures discussed in the previous chapter (Sec. 2). The dopant concentration was about 10^{14} cm^{-3}, the p^+ region thickness was 25 μm, the n^+ region thickness was 10 μm, leaving an n-region active region of about 473 μm. Metalized contacts of titanium were attached to these small diodes and several of them were tested. Figure 16 shows a typical load voltage waveform produced by the UNM diode in the test circuit.

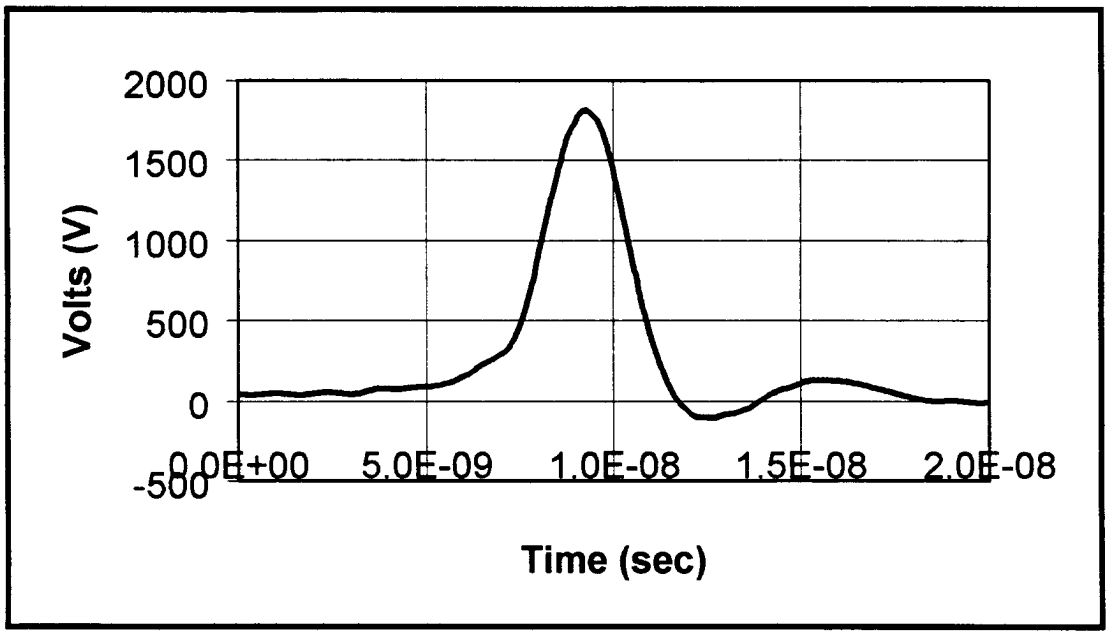

Figure 16. Load response with DSRD Type II and UNM 500 μm peaking diode.

The 10-90 rise time of the pulse in Fig. 16 is approximately 2.4 ns. This should be compared with the rise time of the pulse in the circuit with the DSRD alone, Fig. 5, which exhibits the best rise time measured by this test circuit for a type II DSRD, about 0.75 ns.

The results of the first round of development trials of the fabricated SAS diodes can be summarized as follows. Both sets of devices (both thicknesses) exhibited the typical diode characteristic curve on a Tektronix curve tracer. Dynamic testing of the diodes using the pulsed source (test stand) seemed to point to some improvement in performance over the DSRD alone, as discussed in the previous subsection. This was particularly evident in the reduction of the observed prepulse in the DRSD. The thin devices showed slightly better response over the thick devices. This is attributable to the differing device lengths. Because of available doping sources and materials, doping levels might not have been sufficiently close to what was designed.

Static tests were performed on all devices that underwent dynamic testing. In all cases it was found that, although they still maintained diode characteristics, there were significant changes observed. First, the characteristic curve in the forward direction had less curvature than in the devices that did not undergo dynamic testing. Second, the reverse breakdown voltage was consistently reduced in all devices that had been subjected to dynamic tests. Finally, higher reverse saturation currents were observed.

Optical observations revealed that on some of the devices that underwent dynamic testing the contacts had been blown away. This is attributed to a high current flashover on the surface. Passivation of the surface is presently being pursued to mitigate this.

VII. Commercial Applications for Pulse Sharpener Solid-State Switches

1. Introduction

In order for a new technology to have widespread success, there must be a demand for it above and beyond the military requirements. Therefore, this basic research project required the investigation of possible commercial applications of the fast switch technology reported here. The requirement to perform this work is contained in the second year's tasking to "identify dual-use applications." Of course, the obvious applications for these switches lie with fast, high voltage pulser uses. Some of these that should be considered are:

a. Ultrawideband radar
b. Food preparation/bacteria elimination
c. Collision avoidance mechanisms for vehicles
d. Beacons for search and rescue (SAR)
e. HAZMAT site remediation
f. Pockels cell driver
g. Output switch for gas discharge laser systems

There are many other possibilities as well. Several suggested applications have strong dual-use (military and commercial) potential. For example, ground penetrating radar (GPR), beacons for SAR and HAZMAT uses would be equally important for the DOD and the civilian sector.

The examples above are end use products. What would make the technology reported on here applicable to such uses is the advantage provided by electrically induced high voltage, subnanosecond switching. A survey of a few examples of the use of silicon fast switch technology is discussed below.

2. Ultrawideband Radar

Ultrawideband radar has a host of commercial, as well as, military applications. Mine detection, foliage penetration, mineral deposit location, and geological surveys are just a sample of GPR uses. A recent summary of ultrawideband (UWB) applications is contained in Ref. [22]. In this paper, the requirements for UWB pulser technology in dual-use applications are stated. Short range, medium range, and long range applications are evident.

Some examples of short range pulser applications are laboratory equipment for the assessment of UWB antennas, fast protection devices, system vulnerabilities to UWB radiation and circuit analysis. There is a need for pulsers with output voltages of between millivolts to > 10 kV. Confidence in the repeatability of these pulsers and the need to fire many shots (long lifetimes) is a definite requirement.

Medium range applications include airborne platforms of UWB SAR to detect a variety of small targets on or below the ground surface that may be obscured by vegetation. Another possibility is to operate UWB radars in a bistatic configuration as an intruder alarm that could give detailed information about what has penetrated the protected area. Another medium range application is a collision avoidance UWB radar that could be used on vehicles (cars, boats, rail, etc.) or on aircraft for ground maneuvering while preventing wingtip mishaps.

An UWB radar used in conjunction with standard search and surveillance radar is an example of a long range application that clearly will require very high voltage pulsers to provide sufficient electromagnetic energy at a distance. Another possible use would be space-based UWB radar platforms.

The typical pulse parameters quoted for such uses are 1 – 25 kV, < 200 ps rise time, lifetimes of greater than 10^5 shots, and a pulse repetition rate of approximately 1 kHz. As tested at UNM, the Russian SAS technology would appear to meet most, if not all, of these requirements.

It should also be noted that Grekhov and Kardo-Sysoev have demonstrated the ability to stack DSRDs in such a way as to produce high voltage pulsers [[6], [11]]. Although these circuits were not tested in this research effort, pulsers based on the DSRD and SAS devices have been demonstrated at UNM. In July 1996, UNM tested a PPG-10-5 pulse generator built by Ioffe Institute for the university. The generator specifications were:

Output Voltage:	10,000 V into 50 ohms
Rise time:	< 100 ps with shaping head
Pulse Width:	1 to 2 ns decay
Pulse Repetition Rate:	> 5 kHz
Dimensions:	< 200 x 130 x 100 mm

The make-up of this pulser consisted of one SAS sharpener diode (the so-called shaping head), three DSRDs (type unknown), and 13 blocks of an unspecified number of thyristors. The operation of this pulse generator worked well at lower repetition rates. A sample pulse at 100 Hz measured with a Tektronix SCD-5000 is shown in Fig. 17 without the shaper head attached. The rise time for this pulse is 630 ps with a peak voltage of 10.7 kV. The FWHM for the pulse is about 600 ps. When the SAS diode is used to sharpen this pulse, the result is shown in Fig. 18. The switching time has been reduced to 260 ps, the voltage is still 10.7 kV, and the FWHM is now about 800 ps. Note some distortion in the pulse with the shaper head. The distortion was similar at a higher rep. rate of 6 kHz with more severe degradation in peak voltage and rise time (about a 30% reduction in both without the shaper head, and a 45% reduction with the shaper head). Professor Kardo-Sysoev attributed the distortion to the measurement technique.

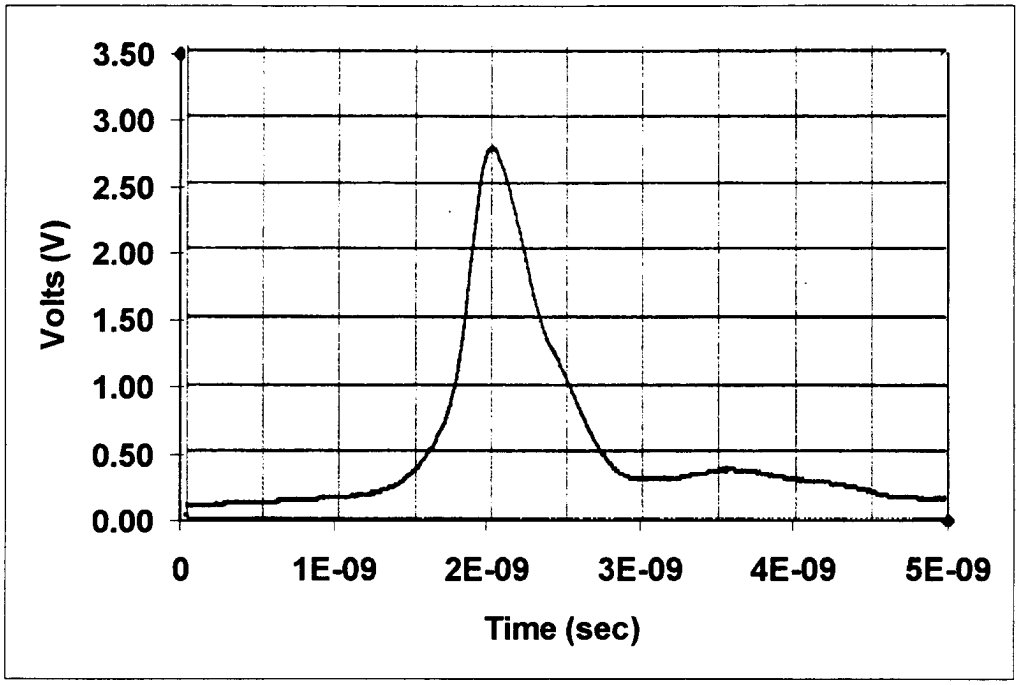

Figure 17. Load voltage versus time at 100 Hz rep. rate for UNM pulser acquired from Ioffe Institute (without shaper head). The scale factor on the vertical axis is 1V = 4000 V.

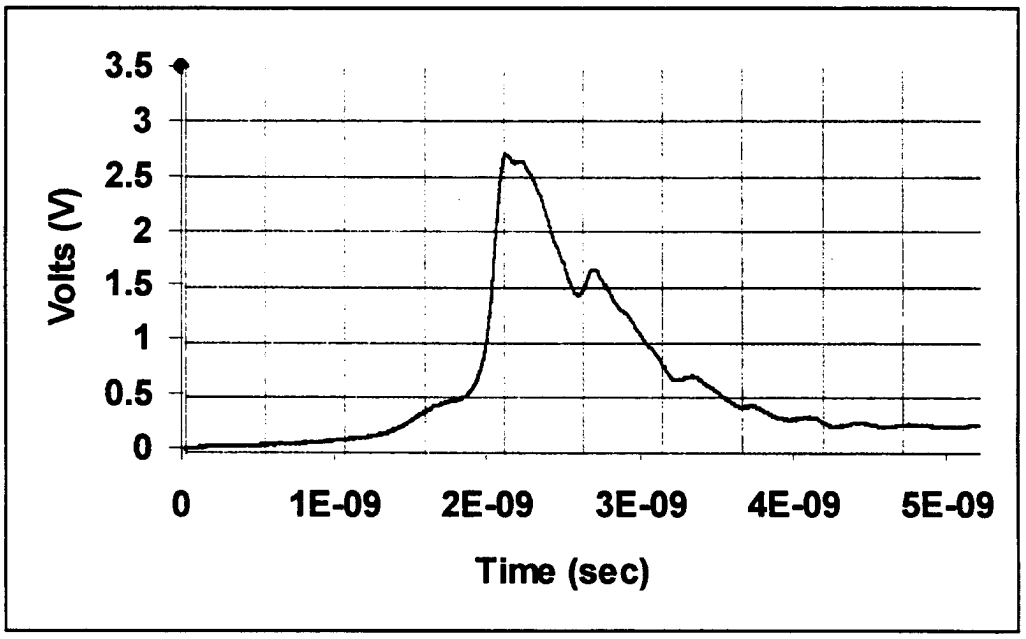

Figure 18. Load voltage versus time at 100 Hz rep. rate for UNM pulser acquired from Ioffe Institute (with shaper head). The scale factor on the vertical axis is 1V = 4000 V.

A proposal [23] was offered to UNM by Dr. Kardo-Sysoev to build a pulser rated at 100 kV with a rise time of less than 1 ns based upon the same technology studied in this

report. This proposal is consistent with designs reported [11] for similar pulsers based upon stacked DSRDs capable of switching 100s of kV in ~ 0.1 ns.

3. Power Switches in Laser Applications

3.1 Pockels Cells

Some types of lasers require very fast, high voltage switching; e.g., ruby, Nd/YAG, and other solid state, active medium lasers. In particular, active Q-switched lasers are high power devices that use electro-optical techniques such as employing Pockels cells [24]. The Pockels cell is used to open and close the optical gate using the refractive index dependence of certain solid crystals under the influence of an electric field.

A check of World Wide Web sites for Pockels cells manufacturing identified two companies in Colorado that make these electro-optical devices. They are:

Meadowlark Optics, Inc.
7460 Weld County Rd. 1
Longmont, CO 80504-9470

Directed Energy, Inc.
2301 Research Blvd., Suite 105
Fort Collins, CO 80526
Phone: (970) 493-1901
Fax: (970) 493-1903
email: deiinfo@dirnrg.com

Meadowlark Optics, Inc. is a designer and manufacturer of passive and electro-optic polarization devices including liquid crystal optics; tunable filters, spatial light modulators, variable retarders, shutters and optical isolators; achromatic and zero-order waveplates, beamsplitting polarizers, pockel cells and dichroic polarizers.

Directed Energy, Inc. (DEI) supplies pulse generators, pulsed laser diode drivers, power MOSFET transistors and other solutions for the generation, delivery and measurement of high power, high fidelity electrical pulses. Applications include test and measurement, lasers, mass spectroscopy, radar, electro-optics and acoustics. Their products include:

High voltage pulse generators and modulators
Pulsed laser diode drivers
Pulsed current sources
High speed/high frequency power MOSFET transistors

The primary applications addressed by DEI's technologies include:

Pulsed high power semiconductor testing

Pulsed burn-in and test equipment for laser diodes
Driving pulsed laser diodes in range-finders, LIDAR and diode-pumped solid-state lasers
Gating/steering ions in Time-Of-Flight Mass Spectroscopy (biotech and environmental research)
Driving acoustic transducers for sonar and non-destructive testing
Driving Pockels cells, Q switches and other electro-optic applications
Pulsed test instruments for dielectric and insulating materials
Burn-in equipment and modulators for Magnetrons
High Power Thyratron Drivers
RF Power Generation
High Frequency Power Conversion

Most, if not all, of these applications are targets for the switches under study in this report. As an example, DEI provides a list of operating parameters for its LDM-SERIES modules which provide extremely fast high current pulses to laser diodes in RANGE FINDER, LIDAR, and other applications requiring high current, very narrow pulses. The rise time, pulse width and amplitude can be configured to values ranging from 3 ns rise time, 6ns pulse width and 20-40 A output to 6 ns rise time, >50 ns pulse width and >90 A output.

A recent report from a Lawrence Livermore Laboratory group [25] is indicative of the interest in an avalanche pulser Pockels cell driver application. In this development, commercially available silicon planar avalanche transistors (from Zetex Inc., part FMMT-417) were used. This component is an npn-type device with a minimum breakdown voltage of 320 V. In their circuit design, three of these transistors were used to produce an inferred electrical performance of less than 100 ps rise time for the last transistor in the chain and a pulse width of one to two microseconds. The output pulse is shown to produce a voltage at the Pockels Cell that peaks at 4 kV for a 10 mm KD*P cell. (The optical rise time is limited to about 1 ns, thus, the transistor rise time must be inferred.) Repetition rates of up to 10 kHz were demonstrated with this design. As a point of reference, the authors report that the transistors used in this application cost between $5-$6 per device.

3.2 Power Conditioning for Gas Discharge Lasers

An early 1990s reference to laser applications suggests that the technology of Grekhov has exciting, new possibilities with regard to gas discharge lasers [26]. In particular, the power conditioning in high-power, pulsed excimer, CO_2, and metal-vapor lasers are suggested as in need of such technology. These lasers have been employed in widespread industrial applications. In order to assure reliable, high-quality performance, close attention to the power conditioning of critical elements is required. One of these elements is the output switch, a key component in long-term reliability. For excimer lasers, the pulses can be tens of kilovolts in amplitude, with rise times a few nanoseconds. For the CO_2 laser, the rise time requirements could be much less. The types of switches

currently employed, the authors report, are spark gaps, thyratron tubes, silicon-controlled rectifiers (SCRs), and magnetic switches. Spark gaps can get to high currents (tens of kA) with a large dI/dt (> 10^{12} A/s), but suffer from slow rep rates (tens/s) and lifetime limitations (10^7 shots or less). Thyratrons have high rep rates (a few kHz) but lower dI/dt. SCRs can operate at very high power levels for a long time, but have very slow rise times (< 10^8 A/s). A magnetic switch in series with the SCR can improve the dI/dt by a factor of ten. Grekhov's new technology, thus, is mentioned as a recent development in solid state switches that "much higher levels of current rise rate and peak current amplitudes are possible" without use of a magnetic switch. This article is anticipating more widespread use of Grekhov's work across the entire spectrum of solid state switches under development (microsecond to subnanosecond regimes) for use in gas discharge laser systems.

4. Recent Russian Switch Developments and Other Applications

Grekhov has recently reported new developments in high power solid-state switches that can produce repetitively pulsed, mega- and gigawatt devices [27]. One type of technology is based upon pulsers built with reversibly switched dynisters (RSD's). Grekhov has been developing RSD pulsers for some time [6], but the power levels now reach in the gigawatt range. These rather large semiconductor switches (8.0 cm) are reported to switch 200 –300 A of current in as little as 50 μs. Switching greater than 1.0 MA of current with all solid-state switches now appears possible. Such pulsers have wide applications in laser pumping, waste water treatment and industrial gas cleaning. For example, a pulser based on one RSD has been tested for water purification purposes which produces 40 J per pulse, 250 Hz, at 30 kV.

The author also suggested that there is a potential application for this technology in the U. S. National Ignition Facility (NIF) program as a power source for the NIF lasers. Discussions are currently being held to determine the feasibility of using Grekhov's RSD's in the NIF.

A new type of diode was also reported by Grekhov called an inverse recovery (IR) diode. This is a new mode of fast recovery similar to the DSRD. This newer technology has promise for delivering higher energy per pulse than a DSRD while still maintaining the fast recovery times of a DSRD, i.e., the nanosecond regime. Grekhov has built the first nanosecond pulser built with IR diodes. It is a 30 kV pulser with a rise time of 3 ns, a repetition rate of 1 kHz, 2 kA current. The IR diode stack consists of 15 diodes that each have a 1 cm diameter.

Finally, a new company in Colorado, UltraLaser, has a current, active interest in using low voltage DSRDs developed by the Ioffe Institute group [28]. This company heard of the Russian fast switches through the published work of this research project. The DSRDs are proposed to be used to build a small laser that will be employed in the processing of silicon wafers. In this application, the DSRD stack must supply 1.3 kV in less than 200 ps with a pulse width of about 500 ps. In addition, the repetition rate required is 1 MHz and the device must operate for thousands of hours without failure. The current proposal is to do this with 200 V DSRDs. The Russians believe that they can

reduce the rise time to 200 ps with this modest voltage at the very high rep. rate needed. This would be a breakthrough in solid state technology. The footprint of the entire laser is quite small (no more than a few cubic inches) and the pulser must attach directly to the laser to keep the capacitive coupling to a minimum. Note that this circuit will not have an SAS shaper head with it. This is apparently due to the inability of the SAS to withstand the Joule heating at this very high frequency. Lifetime requirements may also be a factor. Such small pulsers built with stacks of low voltage DSRDs may have some utility in HPM ultra wideband technology.

VIII. Conclusions and Recommendations

This study met all of the original objectives. Russian silicon switch technology was investigated to validate the performance parameters of (DSRDs) and silicon avalanche shapers (SASs). The Russian theory of operation for the SAS was examined and alternative theories were offered due to inconsistencies with actual operational data and numerical simulations.

A new design for the SAS was offered based upon the information gathered in this study. This design was fabricated at the University of New Mexico. The preliminary results were that the devices displayed diode characteristics and resulted in some minor pulse sharpening. Passivation of the device to inhibit flashover was found to be a critical issue. There was insufficient time to attempt to fabricate additional sets of devices to validate the proposed models; however, there was nothing in the results that were found to be inconsistent with the understanding developed in this work.

1. Conclusions

Specific conclusions reached in this three-year study are:

a. *Regarding the operation of the Russian diodes:* the DSRD and SAS operate with parameters as suggested by the manufacturer (Ioffe Institute).
   1.) The DSRDs tested met, or exceeded, the switching times for the voltages indicated by Ioffe personnel.
   2.) Although the SASs did not turn off in the advertised time interval (450 ps vs < 100 ps), this was attributed to the fact that the test circuit employed was not able to reach the optimum *dV/dt* for its operation, 2×10^{12} V/s.
   3.) Lifetimes of the devices exceeded 10^{11} shots with no apparent degradation.

b. *Regarding the theory of operation of the SAS:*
   1.) The theory of operation of the SAS offered by Grekhov and his colleagues are not consistent with the observed laboratory results and numerical simulations.
   2.) The SAS operates in a manner tha is more consistent with TRAPATT operation rather than based upon instantaneous breakdown of the active n-region.

c. *Regarding the design of fast closing switches which employ avalanche breakdown:*
   1.) The length of the n-region for the SAS will depend on the dopant concentration and the desired level of punch through and should be determined by using Eq. (1) or preferably the results of numerical modeling.
   2.) The length of the p^+- and n^+-regions for the SAS did not seem to be a factor in the numerical analysis of the SAS but should be much greater than the anticipated SCR thickness in these regions and also thick enough so that the post-metallization anneal does not allow metal to diffuse near either junction.

3.) The area of the SAS will depend on the required power handling capability. For pulse sharpening applications the current flowing through the device will be determined by the load resistance.
4.) The proper design of a SAS-type pulse sharpening diode must start with the desired operating parameters. The *dV/dt* of the input pulse must be sufficient to create the required initial current density (Eq. (11)) for the rapid transition mode of operation.
5.) The SAS diode geometry combined with the *dV/dt* of the input pulse will determine the time delay before breakdown and the disparity between the input and load voltage at this time.

d. *Regarding the manufacture of fast closing diodes:*
1.) Initial devices displayed appropriate diode characteristics.
2.) Passivation was found to be a critical issue for lifetime and reproducibility.

2. Recommendations

Additional efforts at fabrication and testing could lead to validation of the modeling proposed by this study.

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